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EXAMINER	
COLEMAN, ERIC	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/757,516	HANSEN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 8,10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao (patent No. 4,569,016).

3. Hao taught the invention substantially as claimed including a data processing ("DP") system comprising (as to claim 1): A programmable processor comprising: data path an instruction path (path via instruction register to ALU and Mask and rotate logic in figured 2A and 2B); data path (path via general purpose registers and to mask and rotate logic and ALU in figures 2A and 2B);external interface (I-cache and D-cache)operable to receive data from an external source (main memory which is external to the CPU 12) and communicate the received data over the data path (e.g. see figs. 1,2); register file (30) operable to receive and store data from the data path and communicate the data stored data to the (e.g., see figs. 2a,2b and col. 23, lines 49-59 and col. 24, lines 10-27),execution unit (42,56) coupled to the data path and operable to decode and executing instructions received from the instruction path(e.g., see col. 24, lines 10-51). Hao also taught in response to decoding a single processor instruction for writing data based on a mask and data contained in at least one register (e.g. see figs. 2a, 2b and col. 25,lines 23-66 and col. 26, lines 3-46), the mask

comprising fields that each correspond to a field of the data contained in the at least one register(e.g., see col. 26,lines 36-46);the execution unit is operable to detect some of the fields of the mask as having a predetermined value to identify corresponding fields contained in the at least one register as write-enabled data fields(e.g., see col. 26, lines 26-46).

4. Hao did not expressly detail causing the write-enabled data fields to be written to a specified memory location. Hao however taught storing the write enabled data fields to a specified register (e.g., see col. 13, lines 7-12) and taught the processor performs rotate operations on data from a general purpose register and returns the result, or portion of the result to a general purpose register or to main storage (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to store the result of the mask and rotate to main storage. The Hao system stores results in main storage and this would have reduced the number of registers needed to perform further processing.

5. As per claim 2, Hao taught each of the fields of the mask has a width of one bit (e.g., see col. 15, lines 39-44).

6. As per claim 3, Hao taught each of the fields of data contained in the at least one register has a width of one bit (e.g., see col. 15, lines 39-44).

7. As per claim 4, Hao writing comprises reading an unaltered field of data from the specified location and writing the unaltered field of data along with the write-enabled data fields of the specified location (e.g., see col. 15, lines 15-44). Therefore one when the operation was performed on data that originated from main memory and was later

stored back to main memory the reading and writing of unaltered words to/from memory would have been performed in the Hao system (e.g., in the Hao system when the storage to storage instructions were used)(e.g., see col. 12, lines 21-54) .

8. As per claim 5, Hao taught the mask is contained in a specified register (e.g., see col. 28, lines 21-54).

9. As per claim 6, Hao taught storing the result a memory location (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to provide the destination memory location in a register such as the instruction register when the destination address an immediate field or another register when the destination was specified using direct or indirect addressing.

10. As per claim 7, Hao taught the architecture comprising a 32-bit architecture (e.g., see col. 8, lines 64-68). Therefore one of ordinary skill would have been motivated to store the data or instructions to memory in specified memory locations comprises a section of memory having a specific width (e.g., 32-bits) and beginning at a specific memory address at least to allow later retrieval of stored data.

11. As per claim 8, Hao taught the predetermined logic value is 1(e.g. see col. 13, lines 6-15).

12. As per claim 10, Hao taught a data processing system comprising bus coupling components in the data processing system (e.g., see figs. 2a,2b) external memory (main memory that is external to the CPU) coupled to the bus (e.g., see figs, 1,2) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor (e.g., see fig. 2) the microprocessor comprising

an instruction path (path via instruction register to ALU and Mask and rotate logic in figured 2A and 2B); data path (path via general purpose registers and to mask and rotate logic and ALU in figures 2A and 2B);external interface (I-cache and D-cache)operable to receive data from an external source (main memory which is external to the CPU 12) and communicate the received data over the data path (e.g. see figs. 1,2); register file (30) operable to receive and store data from the data path and communicate the data stored data to the data path (e.g., see figs. 2a,2b and col. 23, lines 49-59 and col. 24, lines 10-27),execution unit (42,56) coupled to the data path and operable to decode and executing instructions received from the instruction path(e.g,. see col. 24, lines 10-51). Hao also taught in response to decoding a single processor instruction for writing data based on a mask and data contained in at least one register (e.g. see figs. 2a,2b and col. 25,lines 23-66 and col. 26, lines 3-46), the mask comprising fields that each correspond to a field of the data contained in the at least one register(e.g., see col. 26,lines 36-46);the execution unit is operable to detect some of the fields of the mask as having a predetermined value to identify corresponding fields contained in the at least one register as write-enabled data fields(e.g., see col. 26, lines 26-46).

13. Hao did not expressly detail causing the write-enabled data fields to be written to a specified memory location. Hao however taught storing the write enabled data fields to a specified register (e.g., see col. 13, lines 7-12) and taught the processor performs rotate operations on data from a general purpose register and returns the result, or portion of the result to a general purpose register or to main storage (e.g., see col. 12,

lines 42-60). Therefore one of ordinary skill would have been motivated to store the result of the mask and rotate to main storage. The Hao system stores results in main storage and this would have reduced the number of registers needed to perform further processing.

14. As per claim 11, Hao taught each of the fields of the mask has a width of one bit(e.g., see col. 15, lines 39-44).

15. As per claim 12, Hao taught each of the fields of the data contained in the at least one register has a width of one bit (e.g., see col. 15, lines 39-44).

16. As per claim 13, Hao writing comprises reading an unaltered field of data from the specified location and writing the unaltered field of data along with the write-enabled data fields of the specified location (e.g., see col. 15, lines 15-44). Therefore one when the operation was performed on data that originated from main memory and was later stored back to main memory the reading and writing of unaltered words to/from memory would have been performed in the Hao system. have been performed in the Hao system such as when the storage to storage instructions were used (e.g., see col. 12, lines 21-54) .

17. As per claim 14, Hao taught the mask is specified in a register (e.g., see col. 28, lines 21-54).

18. As per claim 15, Hao taught storing the result in a memory location (e.g., see col. 12, lines 21-60). Therefore one of ordinary skill would have been motivated to provide the destination memory location in a register such as the instruction register

when the destination address an immediate field or another register when the destination was specified using direct or indirect addressing.

19. As per claim 16, Hao taught the architecture comprising a 32-bit architecture (e.g., see col. 8, lines 64-68). Therefore one of ordinary skill would have been motivated to store the data or instructions to memory in specified memory locations comprises a section of memory having a specific width (e.g., 32-bits) and beginning at a specific memory address at least to allow later retrieval of stored data.

20. As per claim 17, Hao taught the predetermined value is 1(e.g. see col. 13, lines 6-15).

21. Claims 9,18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao applied to claims 1-8,10 above, and further in view of Kabir (patent No. 5,933,160).

22. As per claim 9, 18 Kabir taught in response to decoding a second single instruction specifying a register containing a plurality of floating point operands and another register containing a second plurality of floating point operands ; multiplying the plurality of floating point operands in the register by the plurality of operands to produce a plurality of products; and providing the partitioned field of a result as a concatenated result (e.g., see fig. 4, 5a, 5b and col. 8,lines 21-45).

23. It would have been obvious to one of ordinary skill to combine the teachings of Hao and Kabir. Both references were directed toward performing operations of partial widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for

performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Hao system at least to provide the capability use in addition applications such as graphics applications.

24. Claims 19-23,26-30, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao.

25. As per claims 19,26 Hao taught a programmable processor comprising: : data path an instruction path (path via instruction register to ALU and Mask and rotate logic in figured 2A and 2B); data path (path via general purpose registers and to mask and rotate logic and ALU in figures 2A and 2B);cache (I-cache and D-cache)operable to retain data from an external interface and data path (e.g. see figs. 1,2); register file (30) operable to receive and store data from the data path and communicate the data stored data to the (e.g., see figs. 2a,2b and col. 23, lines 49-59 and col. 24, lines 10-27). Hao taught execution unit coupled to the instruction and data paths that is operable to execute instructions received from the instruction path,(e.g. see figs. 2a,2b and col. 25,lines 23-66 and col. 26, lines 3-46), and performing a bitwise insert operation operating on a first operand and a second operand stored in the at least one register (e.g., see col. 26, lines 36-46); and for each bit in the first operand, the bitwise insert operation inserting the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value (e.g., see col. 15, lines 39-44). As to the external interface Hao taught a bus units that interface system bus and other buses that transfer data to /from the CPU via the cache and

which are external to the CPU (12)(e.g., see fig. 1). Also one of ordinary skill would have been motivated to store data in the interfaces at least to provide flexlible timing of the transfer of data between the system bus or other external buses and the instruction bus , internal bus or memory bus. Also, Hao did not expressly detail a virtual memory addressing unit. However as to the virtual addressing unit the use of virtual addressing to a memory was well known in the art at the time of the claimed invention allowing the system to more efficiently address memory when plural tasks were being processed. Therefore one of ordinary skill would have been motivated to incorporate a virtual memory addressing means at least to allow for the simultaneous processing of multiple tasks while simplifying the addressing of storage locations.

26. As per claim 20,27, Hao taught the first predetermined value is a logic 1 (e.g. see col. 13, lines 6-15).

27. As per claim 21,28 Hao taught for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding bit in the second operand has a second predetermined value (e.g., see col. 15, lines 39-44).

28. As per claim 22,29, Hao taught the second predetermined value is 0 (e.g. see col. 13, lines 6-15).

29. As per claim 23,30, Hao taught the destination value is stored into memory (e.g., see col. 12, lines 42-60).

30. Claims 24,25,31,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao as applied to claims 19,26 above, and further in view of Kabir.

31. As per claims 24,31 Kabir taught arithmetic operation where operands were stored in registers of 64-bit width (e.g., see col. 8, lines 5-37 and col. 9, line 27-col. 10, line 28 and fig.5A,5B). As to the operand being 64 bit width one of ordinary skill would have been motivated to use data with more bits such as 64, 128 etc to take advantage of the increasing capacity of industry standard memories, data paths and processors at the time of the claimed invention.

32. It would have been obvious to one of ordinary skill to combine the teachings of Hao and Kabir. Both references were directed toward performing operations of partial widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Hao system at least to provide the capability use in addition applications such as graphics applications.

33. As per claim 25, Kabir taught instructions further comprises a plurality of different group floating-point arithmetic operations that arithmetically operate one multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating-point results (e.g., see col. 4, lines 23-61 and col. 7, line 7-col. 8, line 41).

34. As per claim 32, Kabir taught executing a plurality of different group floating point operation that arithmetically operate on multiple floating point operands partitioned in

fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating point results (e.g., see fig. 4, 5a, 5b and col. 8,lines 21-45 and col. 5, lines 6-47 and col. 4, lines 23-64).

Response to Arguments

Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Note: The applicant argues the priority for the instant application includes the '840 patent (and its appendix) and '599 patent (and its appendix) including bitwise masking. The Examiner however contends that the limitations of claims 9,18, 24,25, 31, 32, are not supported by the 840 or 599 patents).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER